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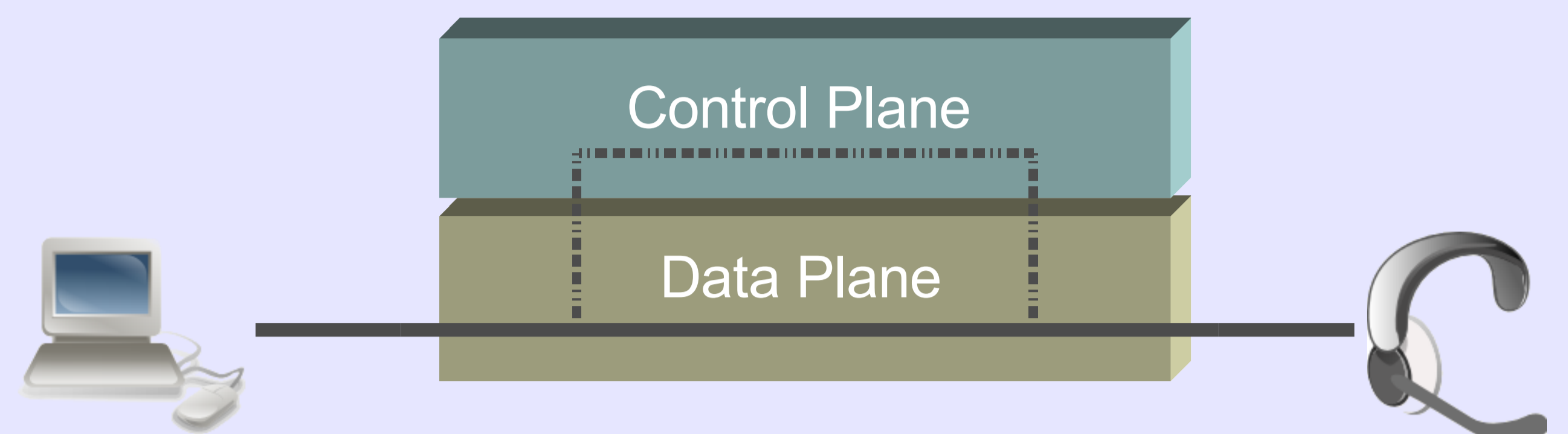
HYBRID NETWORK PROCESSOR ARCHITECTURE

In general, network processors consist of two interworking planes:

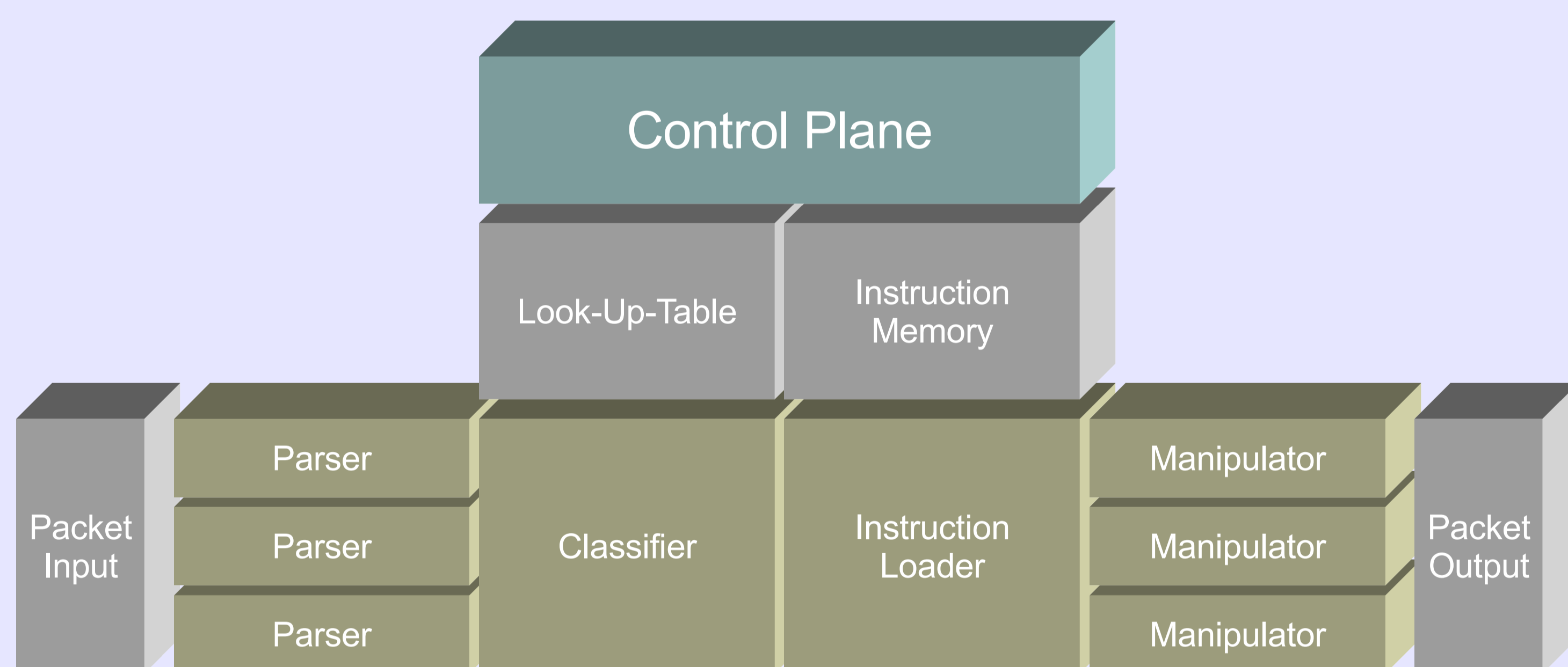
1. Control Plane: higher level algorithms, less deterministic (*Slow Path*) ▶ Software Platform
2. Data Plane: deterministic, lower level packet handling (*Fast Path*) ▶ Hardware Platform

Real-time Transport Protocol (RTP) example

Data traffic is handled autonomously by the Data Plane, while the Control Plane is responsible only for the RTCP (Real-time Transport Control Protocol), limited to 5% of the bandwidth. Hardware acceleration leads to a significant decrease in the software processor workload and bandwidth consumption.



DATA PLANE ARCHITECTURE



- Pipelined architecture
- Classification Look-Up-Table and Instruction Memory act as interface toward Control Plane
- Using C-programmable ASIPs (Application Specific Instruction set Processors) with multi-core support as key components where flexibility is required: parsing and manipulation
- The ASIPs are developed full custom
- Number of cores per pipeline stage is independent using dispatcher/collector per pipeline stage
- Other blocks work at wire rate: packet shifting, classification, checksum verification and instruction loading

FPGA IMPLEMENTATION

- 10GbE (10 gigabit Ethernet) data path processing 20 million packets per second back to back
- Top level bus of 64 bits running at 160 MHz, delivering a bandwidth of over 10 Gbps
- A single ASIP processes a GbE (gigabit Ethernet) stream using a clock frequency of 100 MHz
- The cores are bundled in dual-core entities to optimize resource usage in a Virtex 4 device; five dual-core parsers and five dual-core manipulators handle the requested 10GbE processing bandwidth
- Manual floorplan design is required to achieve timing enclosure
- Interfaces toward external QDRII (Quad Data Rate SRAM) as instruction memory and TCAM (Ternary Content-Addressable Memory) for classification

